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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,148	08/24/2001	Kai-Yeung (Sunny) Siu	SLKN-001/02US	7023

7590 06/01/2005

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EXAMINER	
TRAN, THIEN D	
ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/940,148	SIU ET AL.	
	Examiner	Art Unit	
	Thien D. Tran	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-49 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 26-29 is/are allowed.

6)☒ Claim(s) 1-4,6-10,12-20,22-25 and 30-49 is/are rejected.

7)☒ Claim(s) 5,11 and 21 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 02/12/02, 06/11/02.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 7, 12, 13, 17-19, 20, 22-25, 30-38, 40-43, 45, 46 are rejected under 35 U.S.C. 102(b) as being anticipated by Pan (U.S Patent No. 5,337,308).

Regarding claims 1, 22, Pan discloses a network switch (multi-stage switching system, figure 1), comprising:

an input layer including N input layer circuits (1st Switching stage, figure 1), each input layer circuit including an input layer circuit input port (col.4 line 55) and N queues (N FIFO buffers, figure 2) corresponding to N output terminals;

an intermediate layer including N (K = 1 ... N) intermediate layer circuits (2nd Switching stage, figure 1), each intermediate layer circuit including N buffers (FIFO buffers 31 and 33, figure 2) positioned between N intermediate layer circuit input terminals and N intermediate layer circuit output terminals; and

an output layer including N (L = 1 ... N) output layer circuits (3rd Switching stage, figure 1), each output layer circuit having N output layer circuit input terminals and an output layer circuit output port (figure 5A), said N output layer circuit input terminals

corresponding to individual intermediate layer circuit output terminals of said N intermediate layer circuits (figure 5A).

Regarding claims 2, 23, Pan discloses that each input layer circuit includes: a sorting circuit (self-routing switch 20) to route incoming cells to one of N destinations (col.5 lines 15-19), each destination of said N destinations having a corresponding queue (FIFO buffers) within said input layer circuit (col.5 lines 25-30); and

a transposer circuit (comparator 45 of the output circuit, figure 6) coupled to said N queues and said N output terminals, said transposer circuit being configured to transpose cells stored in said N queues for delivery to said N output terminals (figure 2).

Regarding claims 3, 24, Pan discloses that each intermediate layer circuit includes: a sorting circuit (self-routing switch 32, col.6 lines 30-40) to route incoming cells to said N buffers, said N buffers thereafter delivering said incoming cells to said N intermediate layer circuit output terminals (figure 3).

Regarding claims 4, 25, Pan discloses that each output layer circuit includes: a transposer circuit (sequencer of the output circuit, figure 8) coupled to said N output layer circuit input terminals, said transposer circuit being configured to transpose data cells received at said N output layer circuit input terminals; and

an output layer circuit queue coupled to said transposer circuit and said output layer circuit output port (col.8 lines 35-45).

Regarding claims 7, 19, 38, 40, 42, 45, Pan discloses a network switch, comprising: an input layer to receive a data stream including a set of cells (figure 1), each cell including data and a header to designate a destination device (col.3 lines 5-

10), said input layer including a set of input layer circuits (switch modules, figure 1), a selected input layer circuit of said set of input layer circuits receiving said data stream, said selected input layer circuit including a set of queues corresponding to a set of destination devices (col.5 lines 20-35), said selected input layer circuit being configured to assign a selected cell from said data stream to a selected queue of said set of queues, said selected queue corresponding to a selected destination device specified by said header of said selected cell (col.5 lines 25-35); an intermediate layer including a set of intermediate layer circuits, each intermediate layer circuit including a set of buffers corresponding to said set of destination devices (col.6 lines 1-40), a selected intermediate layer circuit of said set of intermediate layer circuits receiving said selected cell and assigning said selected cell to a selected buffer corresponding to said selected destination device (col.6 lines 1-40); and an output layer including a set of output layer circuits corresponding to said set of destination devices, a selected output layer circuit of said set of output layer circuits storing said selected cell prior to routing said selected cell to a selected output layer circuit output node (co.6 lines 57-65).

Regarding claims 12, 13, 17, 18, 41, 46, Pan discloses that the input layer includes circuitry to identify cell priority values (earliest time stamp values, col.6 lines 25-35) within cell headers.

Regarding claim 20, Pan discloses the layer circuits process cells in accordance with a link skew value and synchronization skew value (time t value, col.7 lines 20-30).

Regarding claim 30, Pan discloses a network switch (multi-stage switching system, figure 1), comprising:

an input layer including N input layer circuits (1st Switching stage, figure 1), each input layer circuit including:

an input layer circuit input port and N queues corresponding to N output terminals (N FIFO buffers, figure 2), a sorting circuit (self-routing switch 20) to route incoming cells to one of N destinations, each destination of said N destinations having a corresponding queue within said input layer circuit (col.5 lines 25-30), and a transposer circuit (comparator 45 of the output circuit, figure 6) coupled to said N queues and said N output terminals, the transposer circuit being configured to transpose cells stored in said N queues for delivery to said N output terminals (figure 6).

Regarding claim 31, Pan discloses that transposer circuit transposes said cells stored in said N queues for parallel delivery to said N output terminals (figure 2).

Regarding claim 32, Pan disclose an intermediate layer including N intermediate layer circuits (figure 1), each intermediate layer circuit including N buffers positioned between N intermediate layer circuit input terminals and N intermediate layer circuit output terminals (figure 3).

Regarding claim 33, Pan discloses an output layer including N output layer circuits (figure 1), each output layer circuit having N output layer circuit input terminals and an output layer circuit output port, said N output layer circuit input terminals corresponding to individual intermediate layer circuit output terminals of said N intermediate layer circuits (figure 1).

Regarding claim 34, Pan discloses a network switch, comprising: an intermediate layer including N intermediate layer circuits (2nd Switching stage, figure 1), each intermediate layer circuit including N buffers (FIFO buffers 31 and 33, figure 2) positioned between N intermediate layer circuit input terminals and N intermediate layer circuit output terminals, said N intermediate layer circuits asynchronously receiving cells at said intermediate layer circuit input terminals and asynchronously delivering cells to said intermediate layer circuit output terminals (figure 1).

Regarding claim 35, Pan discloses that each intermediate layer circuit includes a sorting circuit (self-routing switch 32, col.6 lines 30-40) to route incoming cells to said N buffers, said N buffers thereafter delivering said incoming cells to said N intermediate layer circuit output terminals (figure 1).

Regarding claim 36, Pan discloses a network switch, comprising: an output layer including N output layer circuits (3rd Switching stage, figure 1), each output layer circuit having N output layer circuit input terminals and an output layer circuit output port, each output layer circuit asynchronously receiving cells at said N output layer circuit input terminals and producing a serial cell stream at said output layer circuit output port (figure 1).

Regarding claim 37, Pan discloses that each output layer circuit includes: a transposer circuit (sequencer of the output circuit, figure 8) coupled to said N output layer circuit input terminals, the transposer circuit being configured to transpose data cells received at said N output layer circuit input terminals; and an output layer circuit

queue coupled to the transposer circuit and said output layer circuit output port, said output layer circuit queue producing said serial cell stream (figure 4).

Regarding claim 43, Pan discloses that routing is initiated when said selected queue reaches a specified cell volume level (buffer is used for storing cells, which cells occupy part of the buffer volume).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6, 8-10, 14-16, 39, 44, 47-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan (U.S Patent No. 5,337,308).

Regarding claims 6, 16, 39, 44, Pan discloses limitations of the independent claim. Pan does not disclose an intermediate layer is configured to identify a multicast demand signal in a cell and thereafter replicate said cell to produce a multicast signal. However, it would have been obvious to one having ordinary skill in the art to have to feature of multicast used in the network switch so that same data can be sent to multiple destinations.

Regarding claims 8-10, 47, Pan discloses limitations of the independent claim. Pan does not disclose that selected output layer circuit includes circuitry to generate a flow control warning signal for application to the selected input layer circuit. However, it

would have been obvious to one having ordinary skill in the art to have the feature of generating a flow control warning signal in the network switch so that the network switch routes only high priority data to avoid the congestion as recited in claims 10.

Regarding claims 14, 15, 48, 49, Pan discloses limitations of the independent claim and that the network switch operates in a normal mode. Pan does not disclose the alternately operative in a fault mode to deliver cells to a subset of said intermediate layer circuits. However, it would have been obvious to one having ordinary skill in the art to have the feature of alternately operative in a fault mode to deliver cells to a subset of said intermediate layer circuits so that the network switch is more reliable.

Allowable Subject Matter

5. Claims 5, 11, 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 26-29 are allowed.

Conclusion

7. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Thien Tran whose telephone number is (571) 272-3156. The examiner can normally be reached on Monday-Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu, can be reached on (571) 272-3155. Any inquiry of a general nature

of relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-2600.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have any questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197.

Patent Examiner

Thien Tran

DUC HO
PRIMARY EXAMINER

5-27-05